FIG. 1a

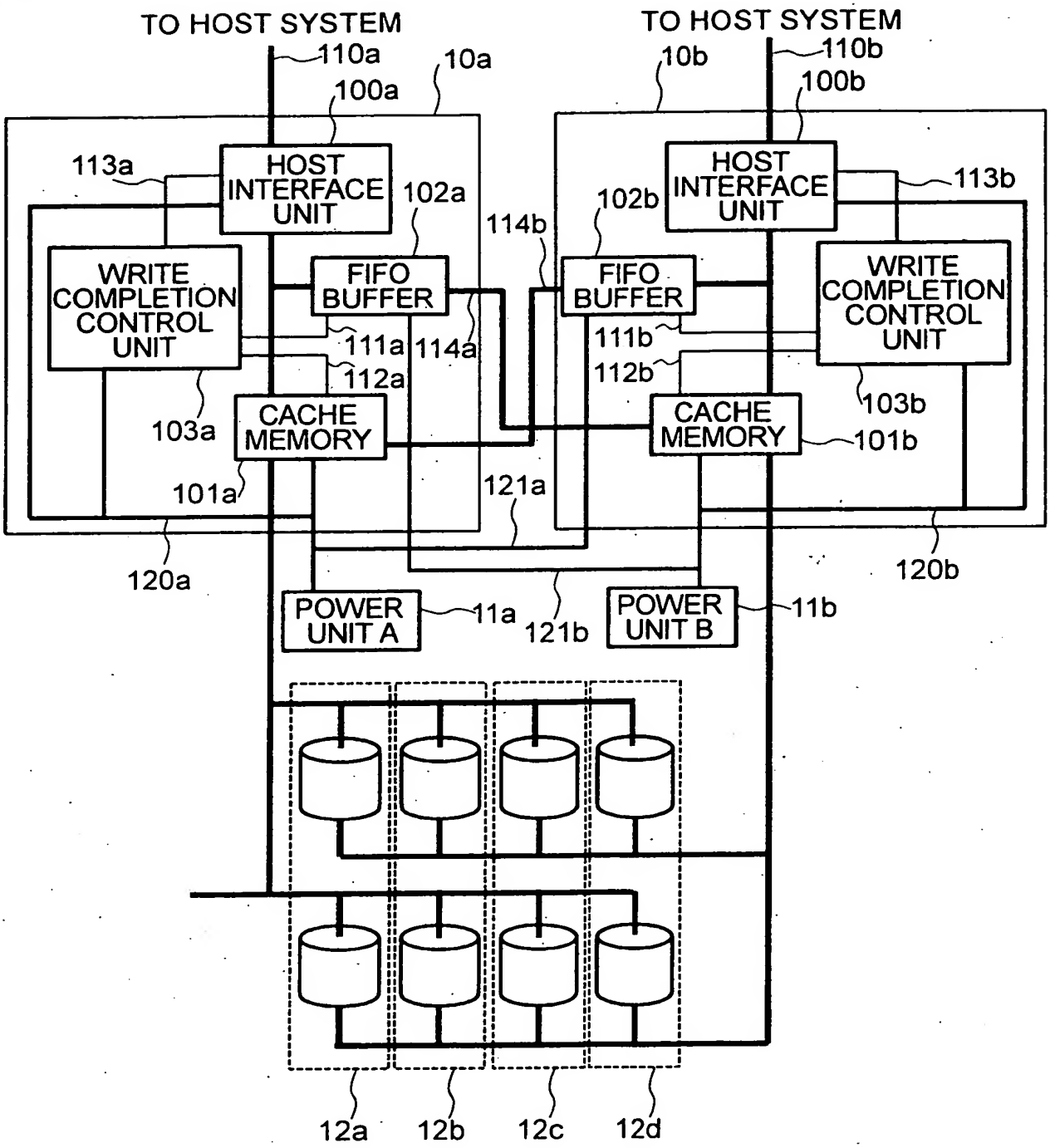


FIG. 1b

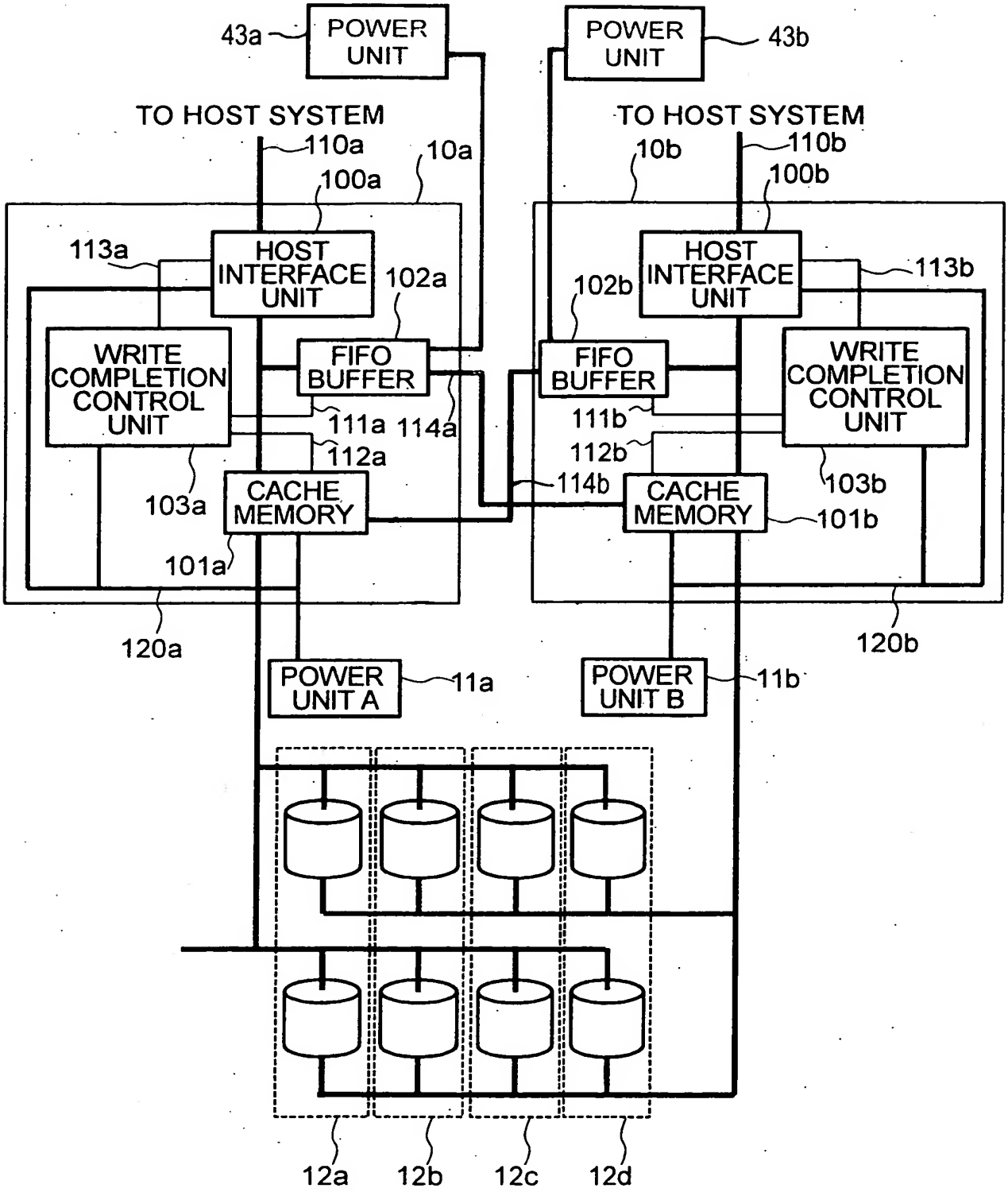

43a
POWER UNIT
POWER UNIT
43b
TO HOST SYSTEM
TO HOST SYSTEM
110a
10a
10b
110b
100a
100b
113a
HOST INTERFACE UNIT
102a
102b
HOST INTERFACE UNIT
113b
WRITE COMPLETION CONTROL UNIT
FIFO BUFFER
FIFO BUFFER
WRITE COMPLETION CONTROL UNIT
111a
114a
111b
112a
112b
103a
CACHE MEMORY
114b
CACHE MEMORY
103b
101b
101a
120a
120b
POWER UNIT A
11a
POWER UNIT B
11b
12a
12b
12c
12d

FIG.2

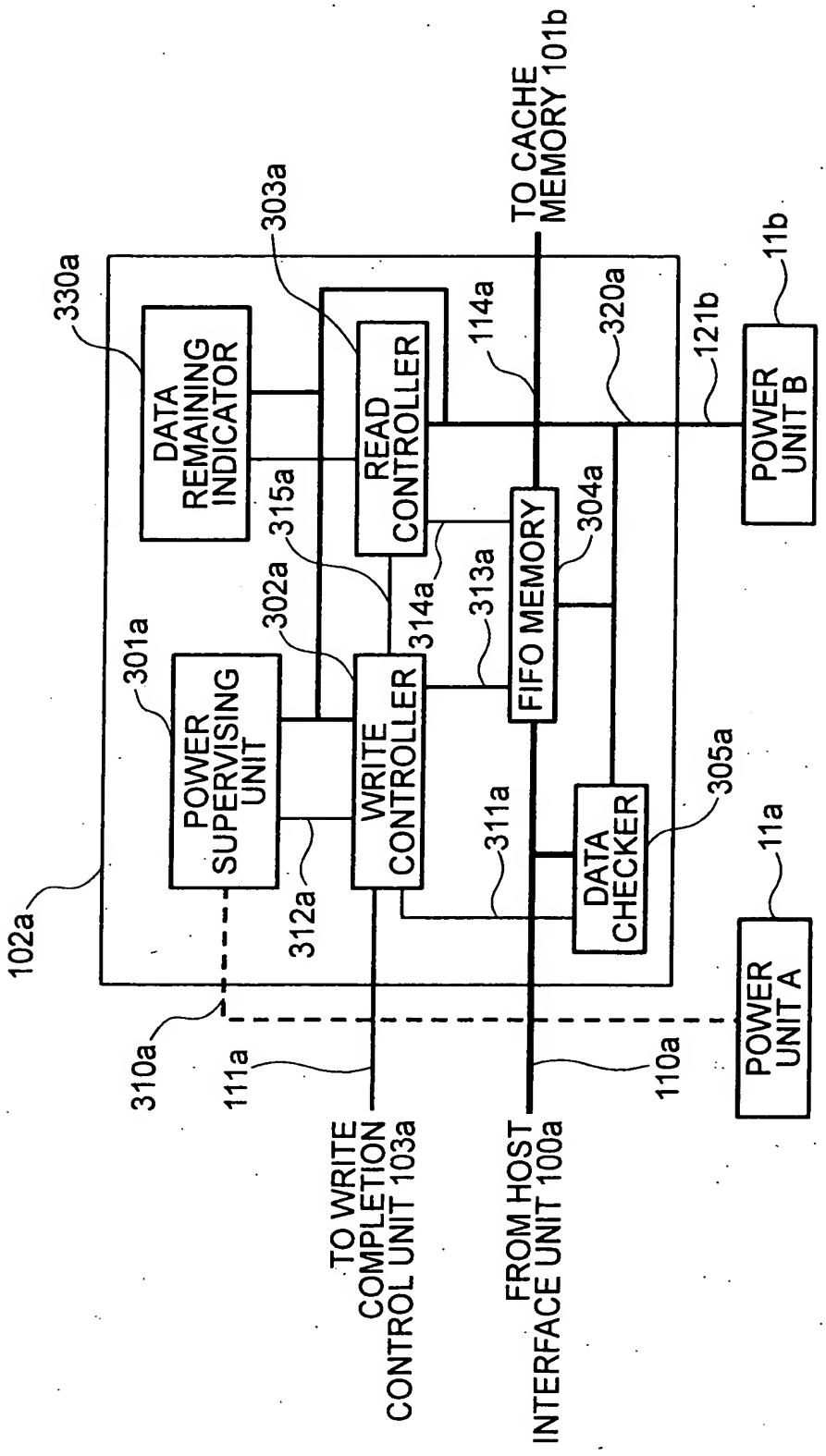

102a
330a
303a
TO CACHE MEMORY 101b
DATA REMAINING INDICATOR
READ CONTROLLER
114a
320a
121b
11b
POWER UNIT B
315a
304a
FIFO MEMORY
313a
314a
302a
301a
POWER SUPERVISING UNIT
WRITE CONTROLLER
311a
DATA CHECKER
305a
11a
POWER UNIT A
312a
310a
111a
110a
TO WRITE COMPLETION CONTROL UNIT 103a
FROM HOST INTERFACE UNIT 100a

FIG.3

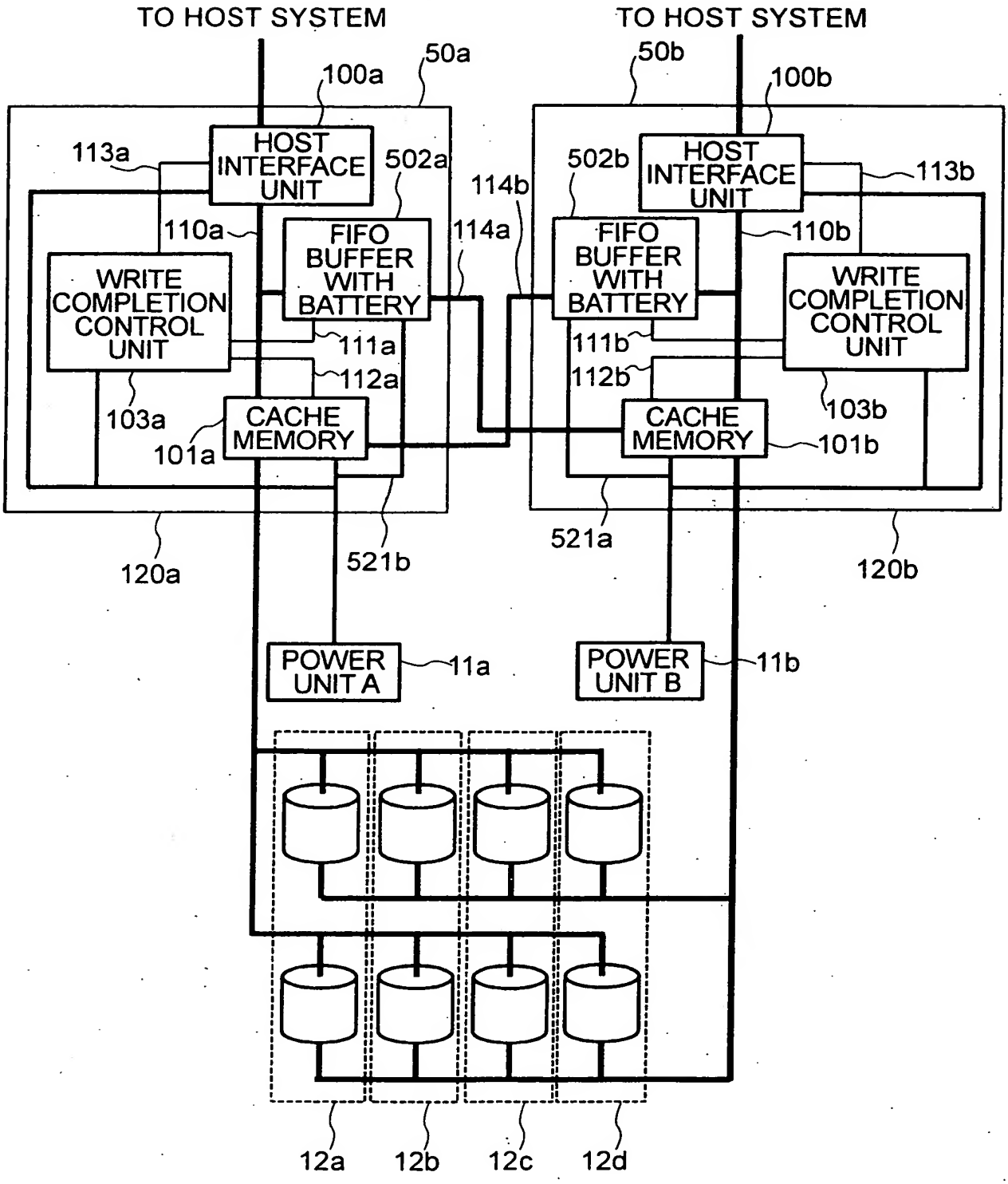
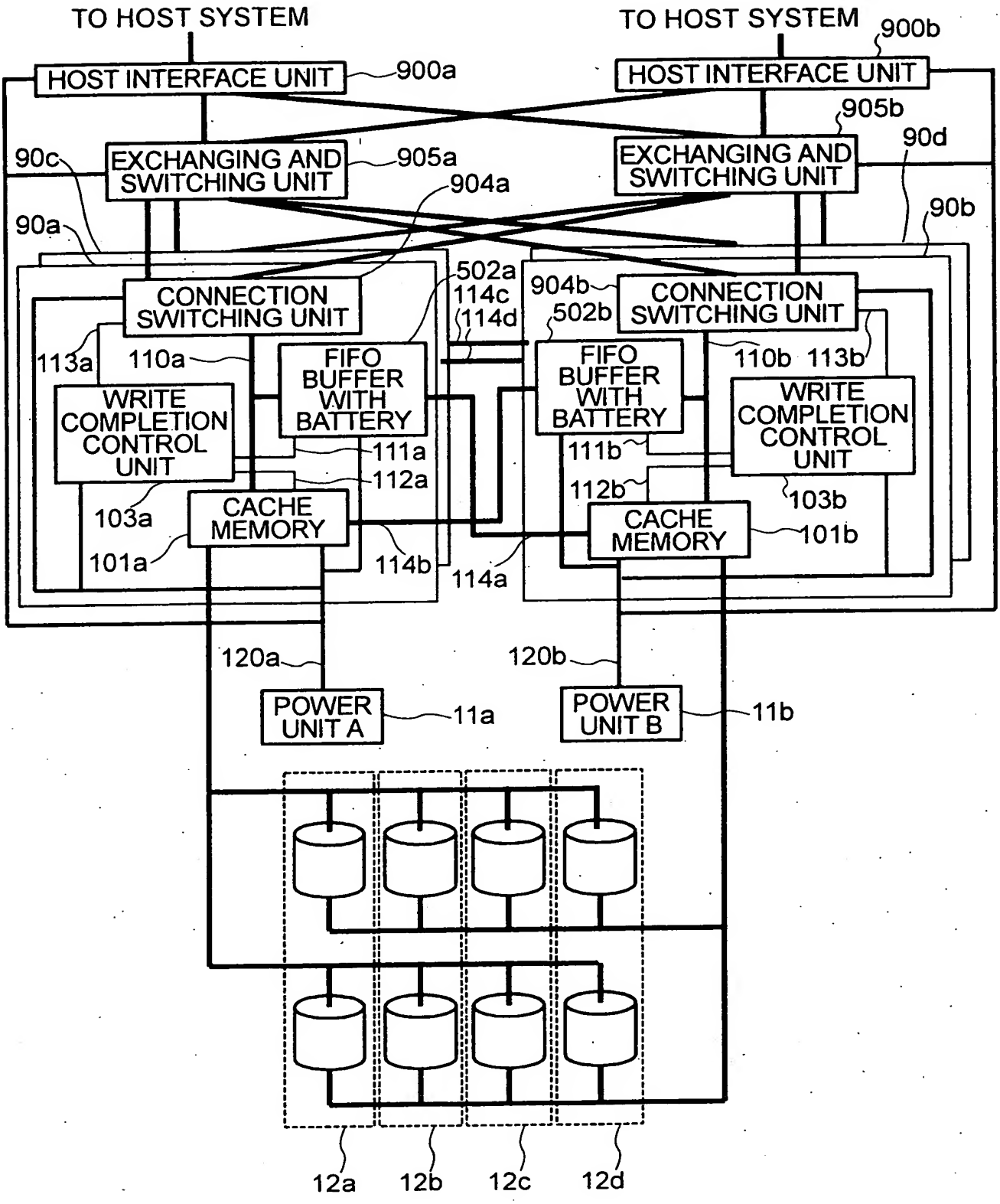

TO HOST SYSTEM
TO HOST SYSTEM
50a
50b
100a
100b
113a
HOST INTERFACE UNIT
502a
502b
HOST INTERFACE UNIT
113b
114b
110a
FIFO BUFFER WITH BATTERY
114a
FIFO BUFFER WITH BATTERY
110b
WRITE COMPLETION CONTROL UNIT
WRITE COMPLETION CONTROL UNIT
111a
111b
112a
112b
103a
CACHE MEMORY
101a
CACHE MEMORY
101b
103b
120a
521b
521a
120b
POWER UNIT A
11a
POWER UNIT B
11b
12a
12b
12c
12d

FIG.7


TO HOST SYSTEM
TO HOST SYSTEM
900b
HOST INTERFACE UNIT
900a
HOST INTERFACE UNIT
905b
90d
90c
EXCHANGING AND SWITCHING UNIT
905a
EXCHANGING AND SWITCHING UNIT
904a
90a
90b
502a
114c
114d
904b
CONNECTION SWITCHING UNIT
502b
CONNECTION SWITCHING UNIT
113a
110a
FIFO BUFFER WITH BATTERY
FIFO BUFFER WITH BATTERY
110b
113b
WRITE COMPLETION CONTROL UNIT
WRITE COMPLETION CONTROL UNIT
111a
111b
112a
112b
103a
CACHE MEMORY
103b
CACHE MEMORY
101b
101a
114b
114a
120a
120b
POWER UNIT A
11a
POWER UNIT B
11b
12a
12b
12c
12d